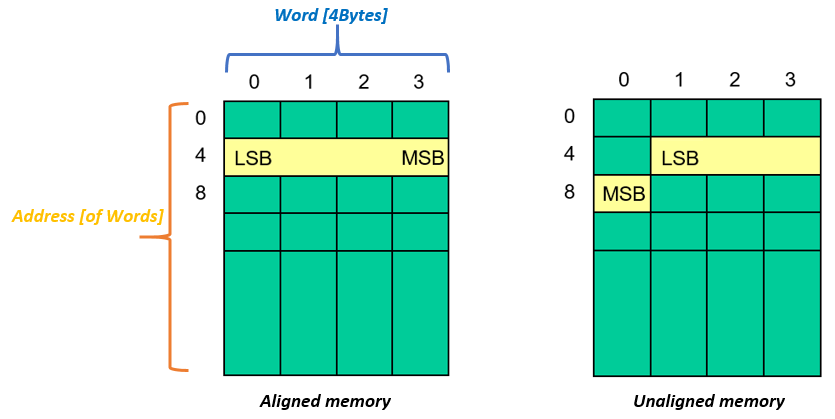
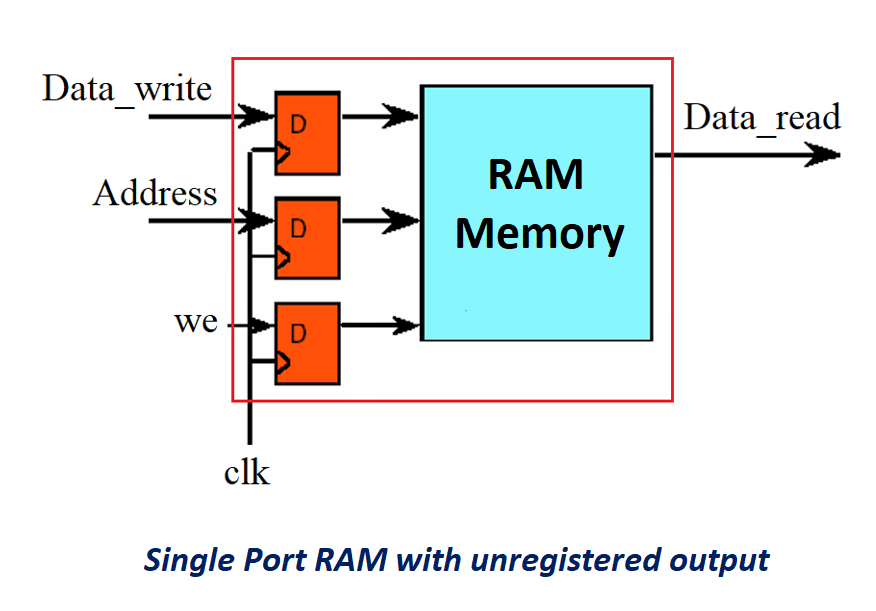
***VHDL\_DUT\_after*** vs. ***VHDL\_DUT\_before***

The difference between ***VHDL\_DUT\_after*** and ***VHDL\_DUT\_before*** designs based on the way we access to a real Alignment Memory. Our case of 32-bit Word alignment, the physical access address is to be padded with 2-bit of zero value, means that (as in ***VHDL\_DUT\_after*** version while the memory access in ***VHDL\_DUT\_before*** is byte access – you can explore the results through their given STP files).

**Note:** the memory access with ***VHDL\_DUT\_before*** design in ModelSim works well (simulation case behaves that each address value associated with a Word).



The given I-Chace (ROM type) and D-Chace (RAM type) memories are 4kB wide each:

